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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,517	07/28/2003	Timothy H. Daubenspeck	BUR920020115US1	1516

23389 7590 09/09/2005

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EXAMINER	
DUONG, KHANH B	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,517	DAUBENSPECK ET AL.	
	Examiner	Art Unit	
	Khanh B. Duong	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-18* is/are pending in the application.

4a) Of the above claim(s) *8-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7 and 16-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This office action is in response to the amendment filed July 11, 2005.

Accordingly, claims 1 and 7 were amended, and new claims 16-18 were added.

Claims 8-15 remain withdrawn from consideration as being directed to a non-elected invention.

Currently, claims 1, 4-7 and 16-18 are active in this application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 4-7 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (FIG. 1; Specification, paragraphs [0014] to [0017]) in view of Cook et al. (U.S. Patent No. 6,022,791).

Re claims 1 and 4-7, the admitted prior art ("APA") discloses in FIG. 1 a crack stop for an integrated circuit (IC) chip having an active circuit area, comprising: the IC chip including a bottom substrate, metal layers (M1 to M4) separated by capping layers 16, a top aluminum layer, and copper metal interconnects 18 in a low-K dielectric material (BPSG); a moisture barrier/edge seal 12 (metal stack: metal lines 22 and via bars 24) positioned along the outer peripheral edges

of the active area 10 of the IC chip; a crack stop formed by at least a metal stack outside of the moisture barrier/edge seal 12 and between the moisture barrier/edge seal and the outer periphery of the IC chip, for preventing damage to the active area 10 of the IC chip caused by chipping and cracking formed along peripheral edges of the IC chip during a dicing operation performed on the IC chip (see Specification, paragraphs [0014] to [0017]).

Re claims 16-18, the APA discloses in FIG. 1 an integrated circuit chip comprising: a bottom silicon substrate; a series of metal layers (M1 to M4) formed above the substrate, each of the metal layers including a low k dielectric material (BPSG) having a dielectric constant less than 4.0, and a copper interconnect 18, said metal layers defining an active circuit area of the integrated circuit chip; a moisture barrier/edge seal 12 forming an inner ring extending around the active circuit area 10 of the integrated circuit, and consisting of a number of metal lines 22 and via bars 24 formed of copper; a top aluminum layer covering said series of metal layers and forming two concentric ring-shaped openings; and a crack stop 14 forming an outer ring extending around the moisture barrier/edge seal 12, and consisting of at least a metal stack located below the concentric ring-shaped openings of the top aluminum layer and on the outer periphery of the integrated circuit chip, said at least a metal stack extending substantially completely between said top aluminum layer and said bottom substrate for preventing damage to the active area 10 of the integrated circuit chip caused by chipping and cracking formed along peripheral edges of the integrated circuit chip during a dicing operation performed on the chip (see Specification, paragraphs [0014] to [0017]). The APA expressly discloses in FIG. 1 the crack stop 14 extends outside of and around the moisture barrier/edge seal 12 and between the moisture barrier/edge seal 12 and an outside periphery of the IC chip.

Re further claims 1, 7 and 17, the claims recite the following product-by-process limitations: "said etched out void regions are formed by a wet etch process" and "interconnects do not form a self-passivating oxide layer". However, these limitations have not been given patentable weight because product-by-process claims are not limited to the manipulations of the recited steps, only the structure implied by the steps. "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Re further claims 1, 6, 7 and 17, the APA discloses the crack stop being formed by at least a metal stack instead of at least a trench or void region that extends substantially completely between the bottom substrate and the top aluminum layer of the IC chip.

Cook et al. ("Cook"), submitted by Applicant in IDS, teaches in FIG. 3d (PRIOR ART) the use of a crack stop comprising a plurality of trenches or void regions 46 that extends substantially completely between the bottom (silicon) substrate and the top final metal or bond pad layer of the IC chip for the purpose of preventing "propagation of delamination cracks initiated in dicing channel 40' in any layer of the structure" [see col. 1, lines 59-62].

Since the APA and Cook are both from the same field of endeavor, the purpose disclosed by Cook would have been recognized in the pertinent prior art of the APA.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the crack stop of the APA in the manner as suggested by Cook because of the desirability to stop propagation of cracks in any layer of the IC chip.

Response to Arguments

Applicant's arguments filed July 11, 2005 have been fully considered but they are not persuasive.

Applicant argues that Cook does not address the specific problem of preventing cracks when a metal stack moisture barrier/edge seal is used in the IC chip. In response, the Examiner respectfully disagrees because the APA addresses in FIG. 1 such specific problem of preventing cracks with a crack stop 14 when a metal stack moisture barrier/edge seal 12 is used in the IC chip. The APA, however, discloses the crack stop 14 comprising a metal stack instead of a deep trench structure. Such deep trench crack stop structure is taught by Cook in FIG. 3d for the same purpose of preventing propagation of cracks into the active area of the IC chip during an IC dicing operation. Thus, it would have been obvious to one having an ordinary skill in the art to modify the crack stop structure of the APA in the manner as taught by Cook.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on Monday - Thursday (9:00 AM - 6:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KBD

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER